

Cover Sheet	1
Block Diagram/Clock Map/Power Map	2-4
Intel LGA775 CPU	5-7
Intel Bearlake- MCH -P31/G31	8-11
Intel ICH7 - PCI & DMI & CPU & IRQ	12
Intel ICH7 - LPC & ATA & USB & GPIO	13
Intel ICH7 - POWER	14
Clock - ICS9LPRS514EGLF	15
<a href="#">LPC I/O - F81182</a>	16
HD- ALC888	17
<a href="#">LAN REALTEK RTL8111C/8111B</a>	18
DDR II System Memory 1 & 2	19
DDR II System Memory 3 & 4	20
DDR II VTT Decoupling	21
PCI EXPRESS X16 & X1 Slot	22
PCI Slot 1 & 2 & 3 Slot	23
IEEE-1394 VT6308	24
VGA Connectors	25
USB Connectors	<a href="#">26</a>
ATX Connetcor Front Panel IDE & SATA Connectors	<a href="#">27</a>
CPU/SYSTEM/POWER FAN	<a href="#">28</a>
ACPI CONTROLLER UPI	<a href="#">29</a>
<a href="#">VRM 11.0 - INTELSIL - ISL6322CR</a>	<a href="#">30</a>
GMCH VCORE &DDR VOLTAGE	<a href="#">31</a>
AutoBOM parts	<a href="#">32</a>

# MS-7392

Version: 2.0

## CPU:

Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

## System Chipset:

Intel - MCH (North Bridge) P31  
Intel ICH7R (South Bridge)

## On Board Chipset:

BIOS -- SPI EEPROM  
[HD Codec -- ALC888](#)  
[LPC Super I/O -- F81182](#)  
[LAN-- REALTEK RTL8111C/8111B](#)  
CLOCK -- ICS9LPRS514EGLF

## Main Memory:


DDR II \* 4 (Max 4GB)

## Expansion Slots:

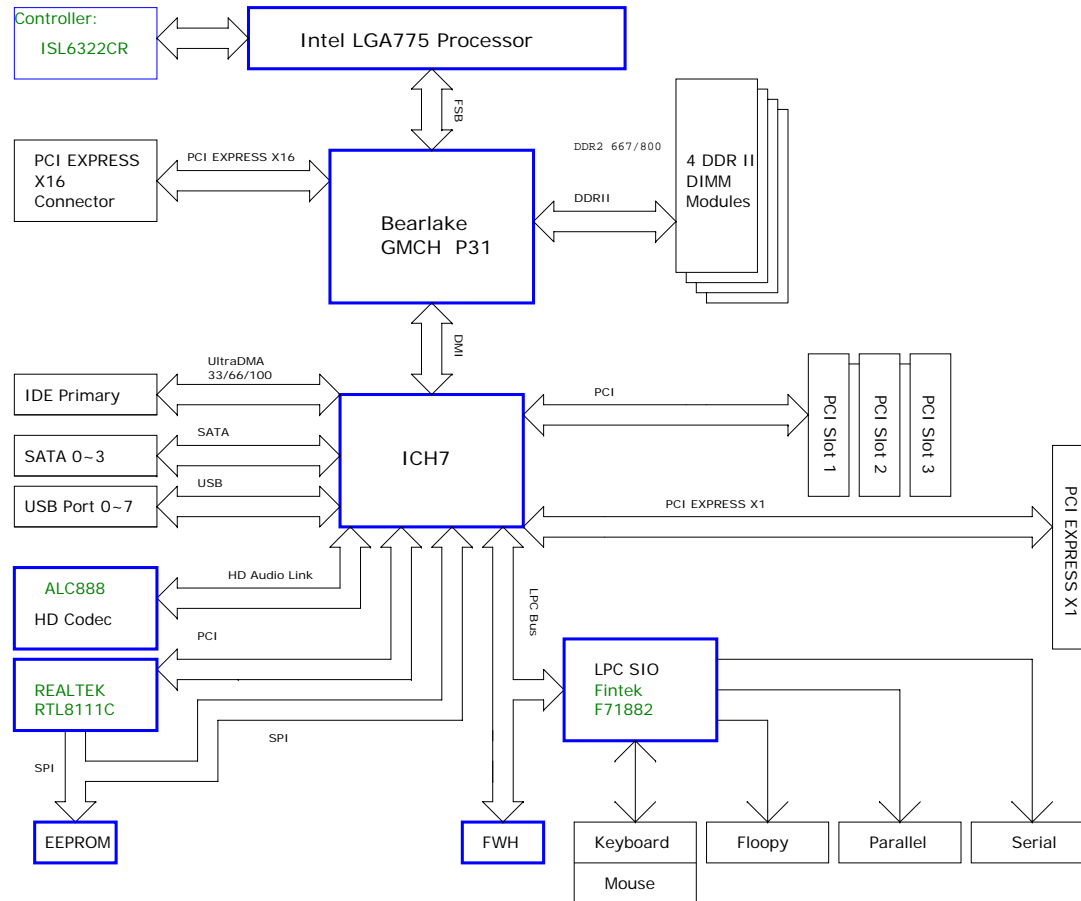
PCI2.3 SLOT \* 3  
PCI EXPRESS X1 SLOT \* 1  
PCI EXPRESS X16 SLOT


## INTELSIL PWM:

[Controller: INTELSIL - ISL6322CR](#)

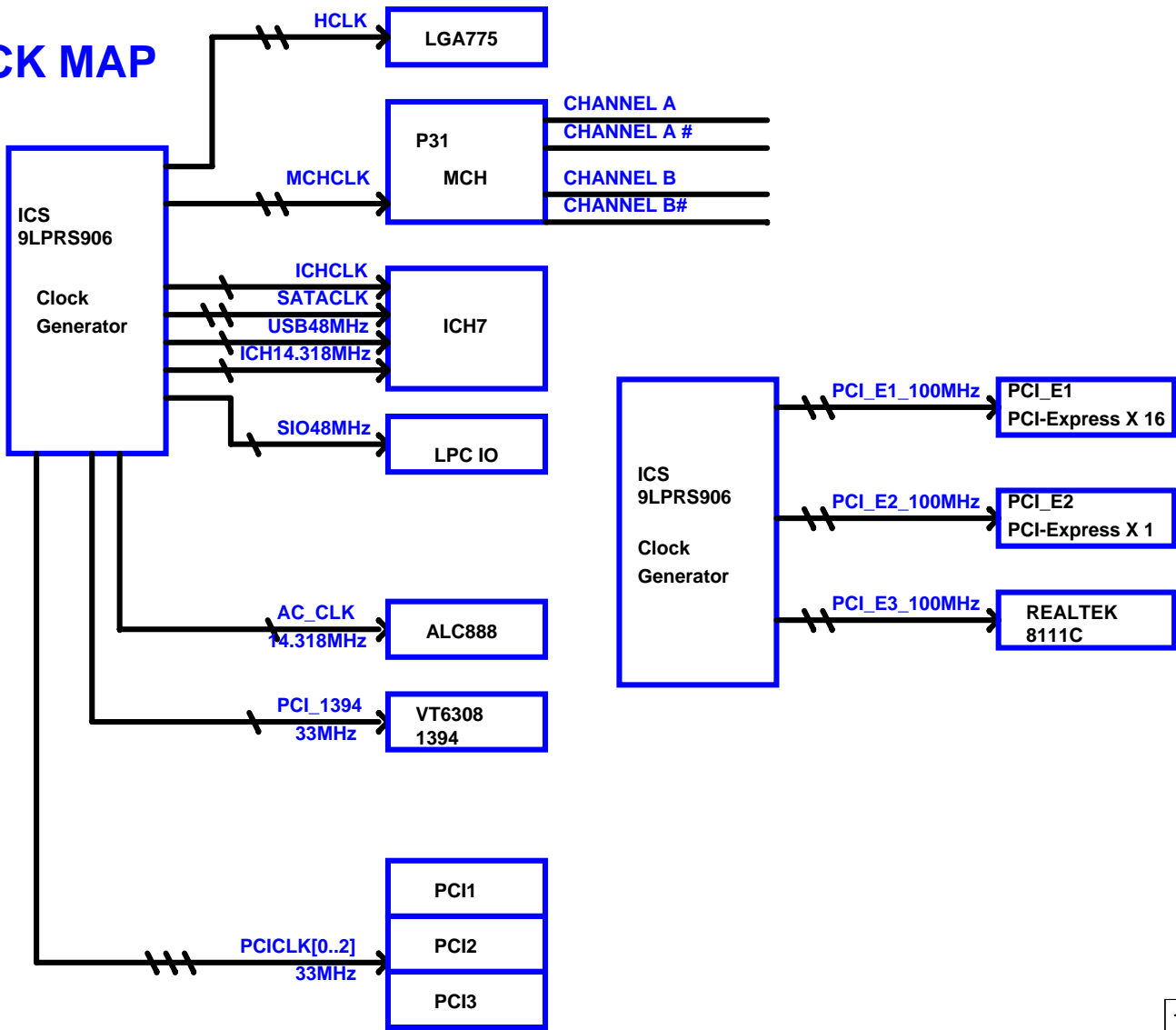
 <b>MICRO-STAR INT'L CO., LTD.</b>		
Title COVER SHEET		
Size	Document Number <b>MS-7392</b>	Rev <a href="#">2.0</a>
Date: Tuesday, August 07, 2007	Sheet 1	of 35

# Block Diagram

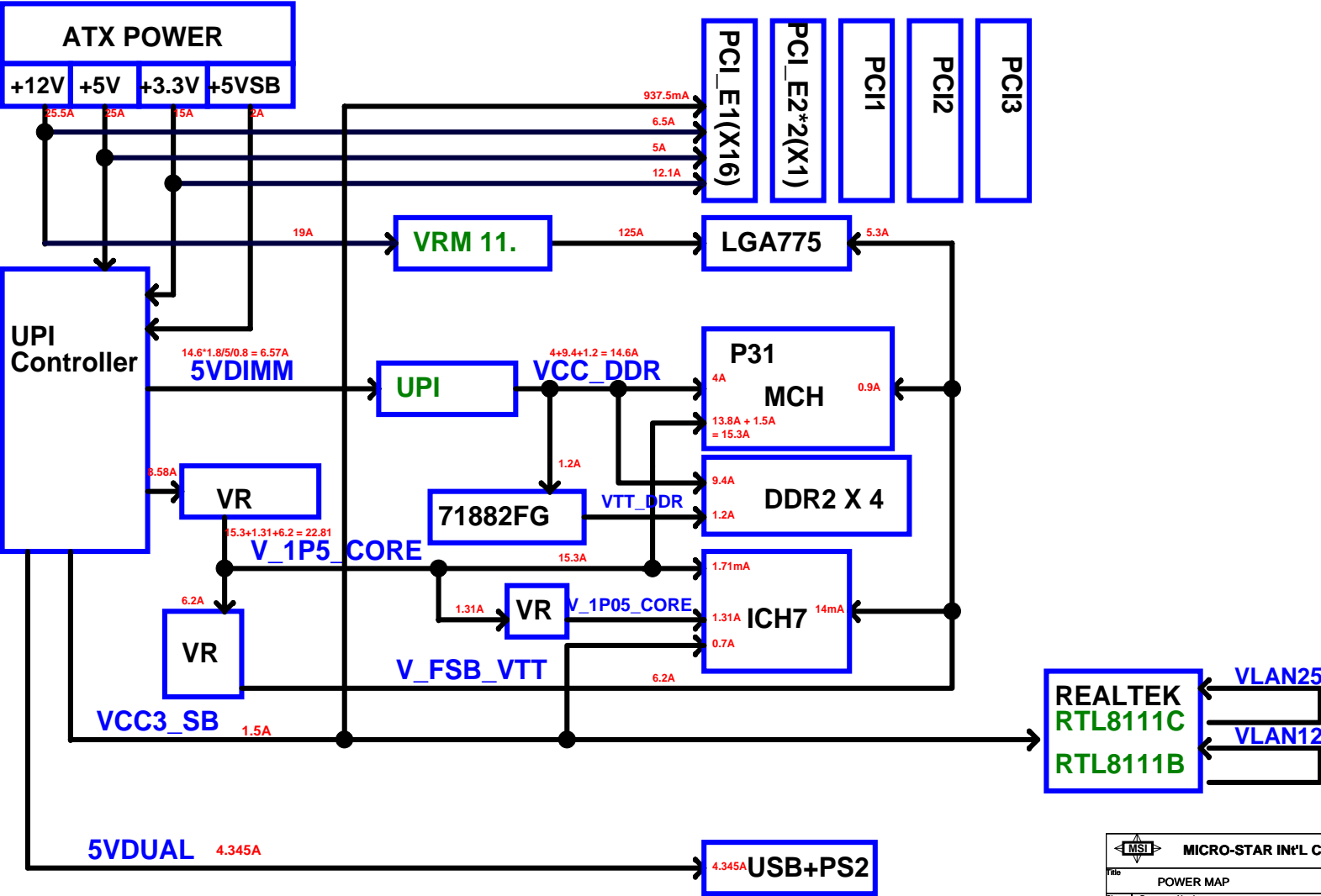


		<b>MICRO-STAR INT'L CO., LTD.</b>	
Title			
BLOCK DIAGRAM			
Size	Document Number		Rev
	MS-7392		2
Date:	Tuesday, August 07, 2007	Sheet	2 of 35

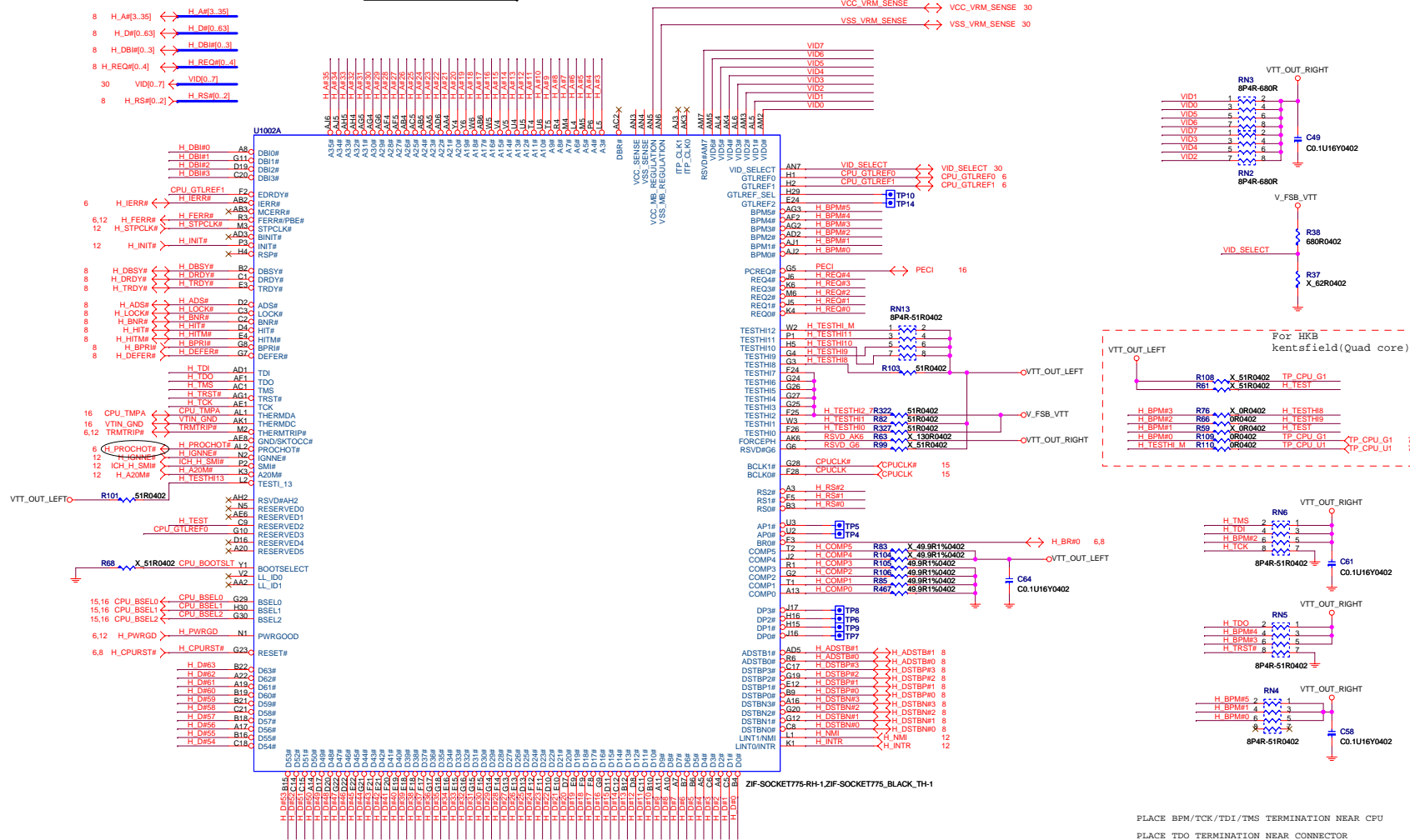
# CLOCK MAP



POWER MAP



### CPU SIGNAL BLOCK




PLACE BPM/TCK/TDI/TMS TERMINATION NEAR CPU  
PLACE TDO TERMINATION NEAR CONNECTOR

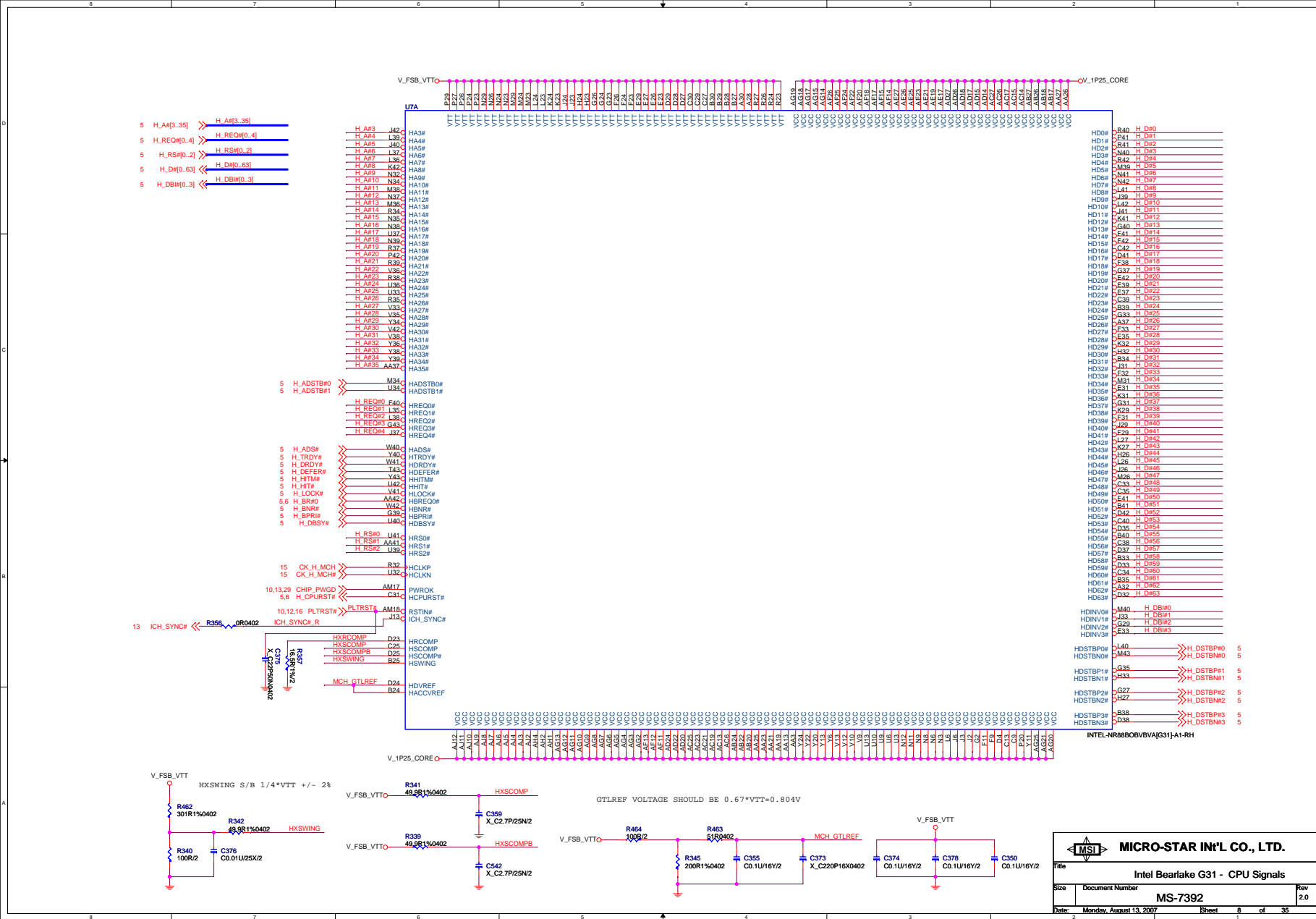


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Title			
Intel LGA775 CPU - Signals			
Size	Document Number	Rev	
	MS-7392	2.0	
Date:	Friday, August 10, 2007	Sheet	5 of 35

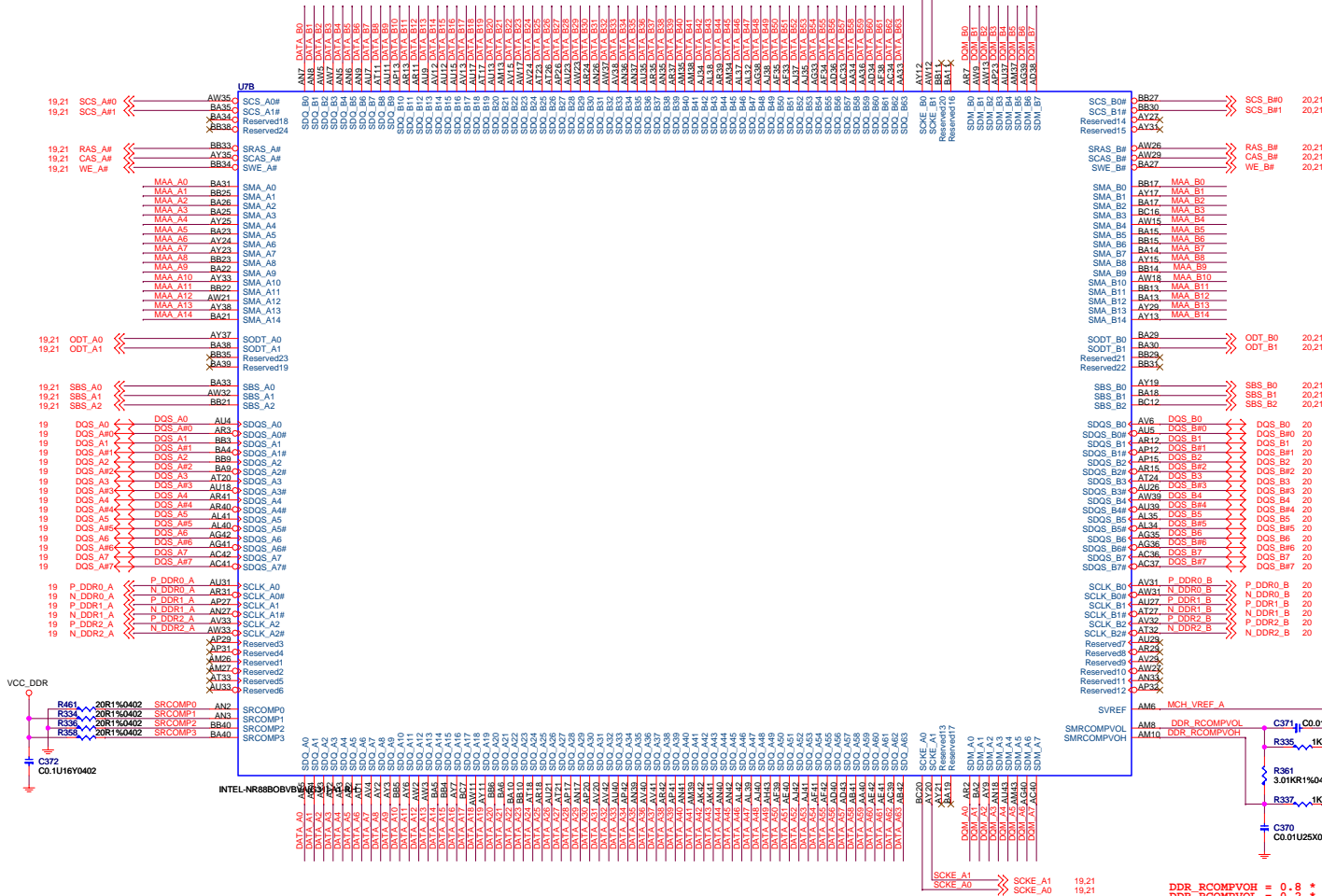


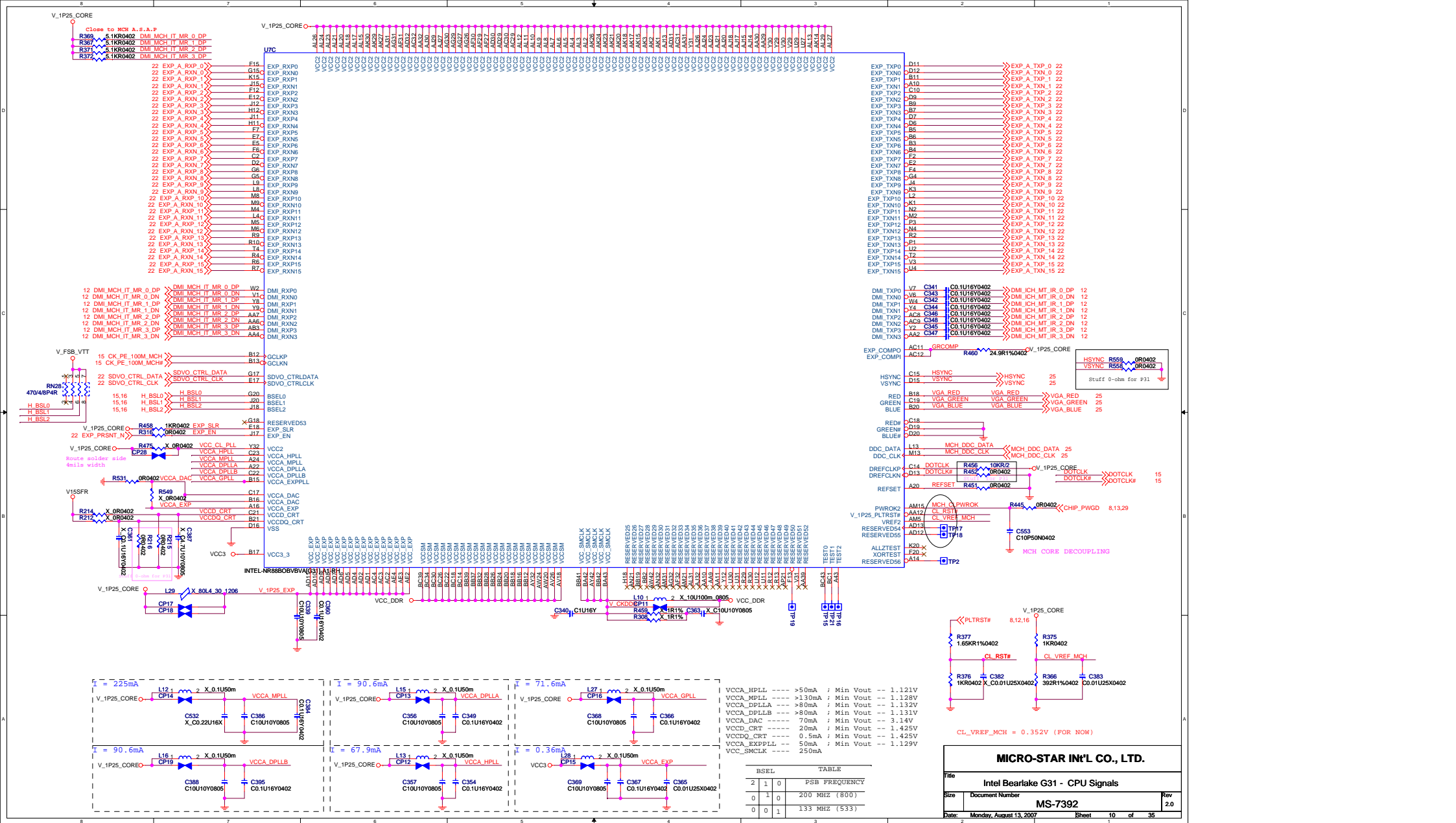
 <b>MICRO-STAR INT'L CO., LTD.</b>			
Title Intel LGA775 CPU - GND			
Size	Document Number	Rev	
	MS-7392	2.0	
Date:	Friday, August 10, 2007	Sheet	7 of 35





20 DATA\_B[0..63] <- DATA\_B[0..63] 20 DQM\_B[0..7] <- DQM\_B[0..7]  
19 DATA\_A[0..63] <- DATA\_A[0..63] 19 DQM\_A[0..7] <- DQM\_A[0..7]  
19.21 MAA\_A[0..14] <- MAA\_A[0..14] 20.21 MAA\_B[0..14] <- MAA\_B[0..14]





VCCA_HPLL	----	>50mA	Min Vout	--	1.121V
VCCA_MPLL	----	>130mA	Min Vout	--	1.128V
VCCA_DPLL	----	>80mA	Min Vout	--	1.132V
VCCA_DPLL	----	>80mA	Min Vout	--	1.131V
VCCA_DAC	----	70mA	Min Vout	--	3.14V
VCCD_CRT	----	20mA	Min Vout	--	1.425V
VCCDQ_CRT	----	0.5mA	Min Vout	--	1.425V
VCCA_EXPPHLL	----	50mA	Min Vout	--	1.129V
VCC_SMCLK	----	250mA			

BSEL			TABLE	
2	1	0	PSB FREQUENCY	
0	1	0	200 MHZ (800)	
0	0	1	133 MHZ (533)	

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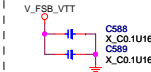
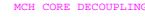
Title: Intel Bearlake G31 - CPU Signals

Size: Document Number

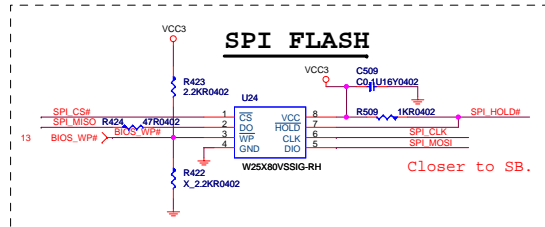
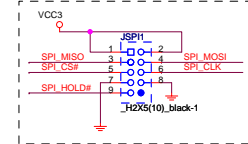
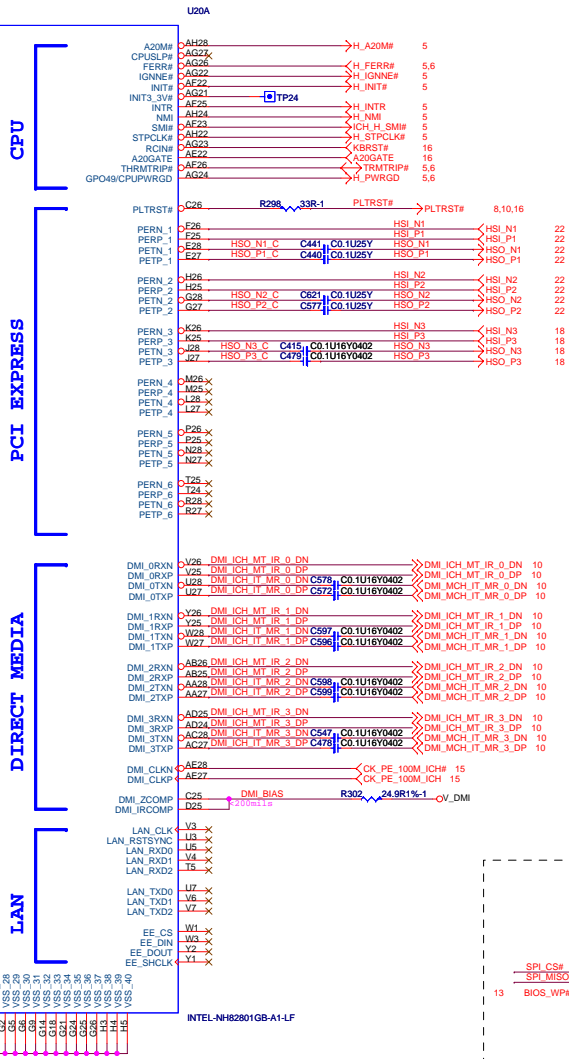
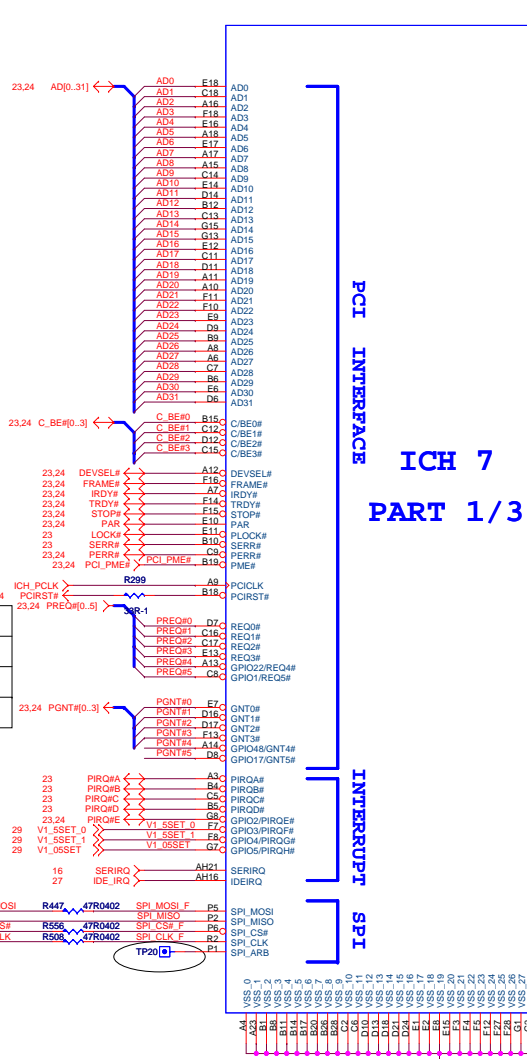
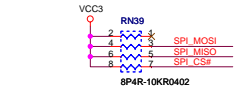
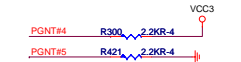
Rev: 2.0

Date: Monday, August 13, 2007

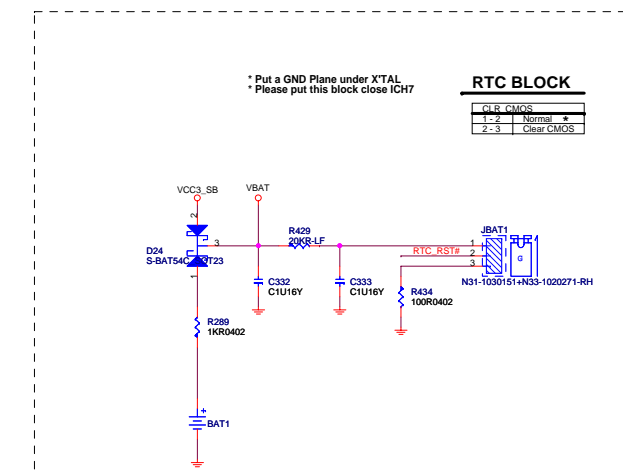
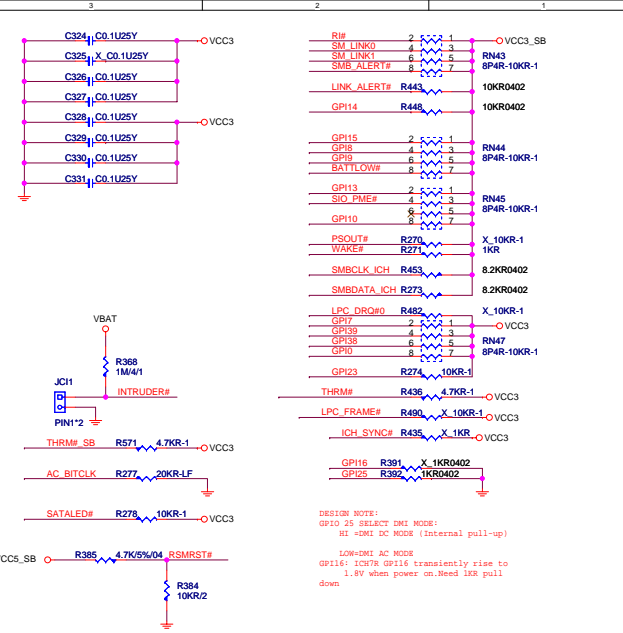
Sheet: 10 of 35



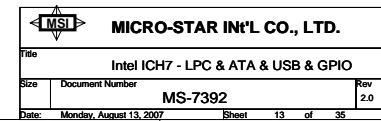
GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC



<b>MICRO-STAR INT'L CO., LTD.</b>		
Title Intel ICH7 - PCI & DMI & CPU & IRQ		
Size	Document Number <b>MS-7392</b>	Rev 2.0
Date	Monday, August 13, 2007	Sheet 12 of 35

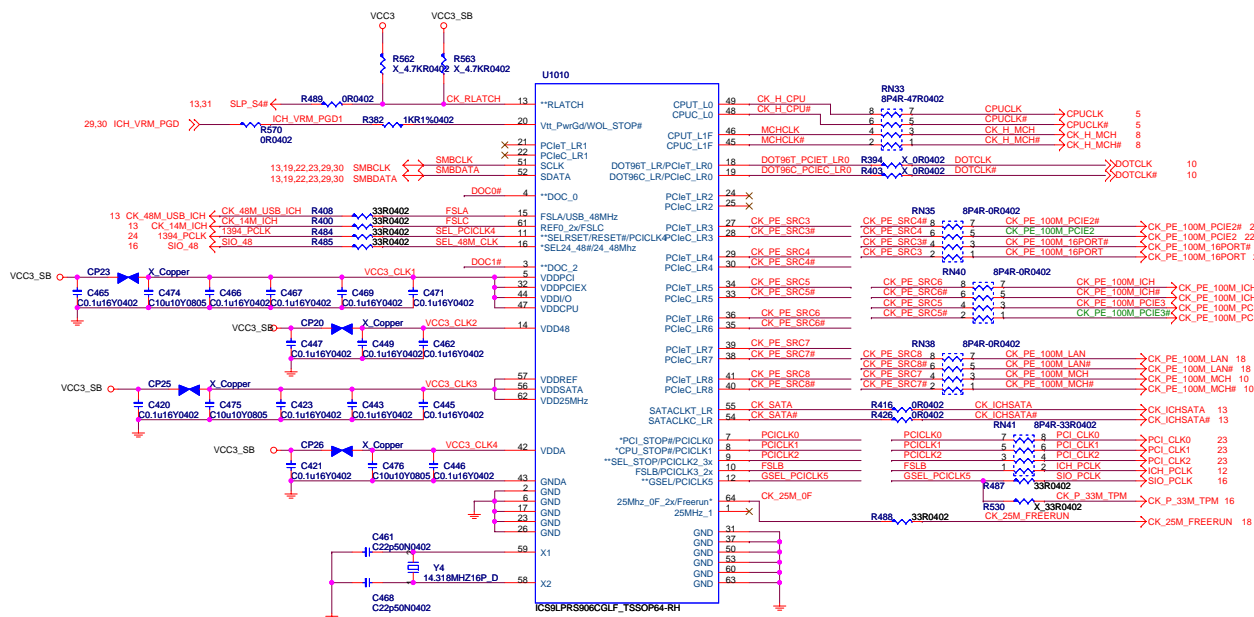


Following are the GPIOs that need to be terminated properly if not used:  
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3\_3 if unused.  
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus\_3 if unused.

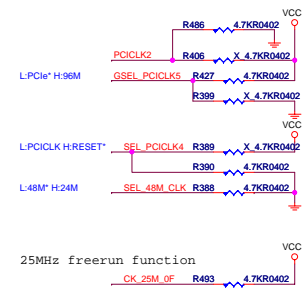




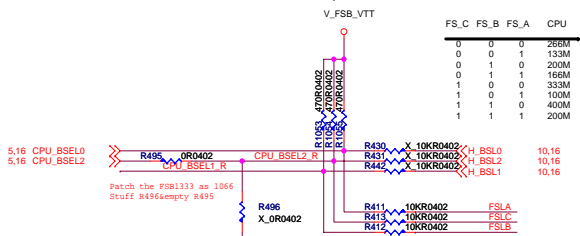
## Clock Generator - ICS9LPRS906CGLF



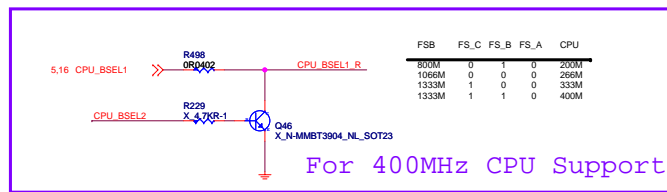
## CLOCK GEN STRAPING



### CPU Frequency Selection

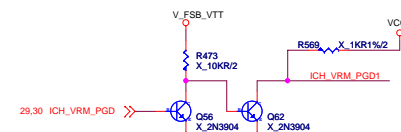
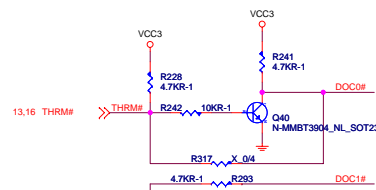


FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	200M

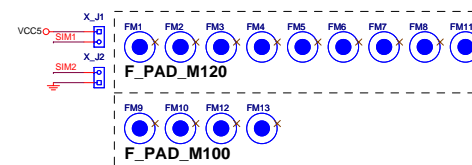
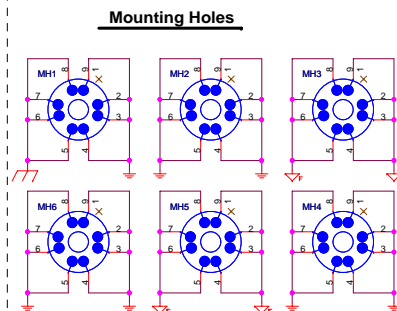


FSB	FS_C	FS_B	FS_A	CPU
800M	0	1	0	200M
1066M	0	0	0	266M
1333M	1	0	0	333M
1333M	1	1	0	400M

## For 400MHz CPU Support



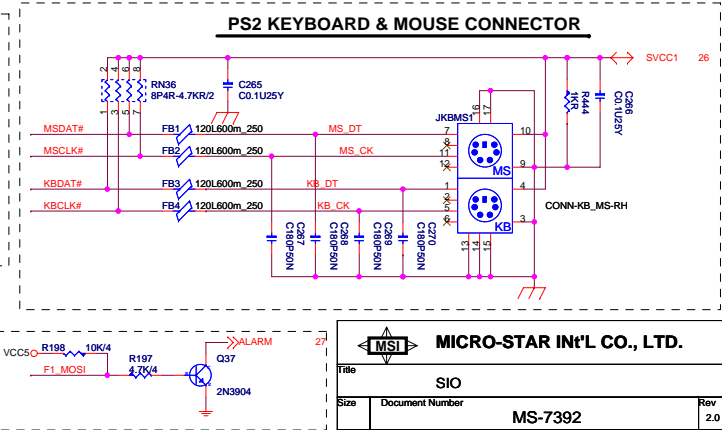
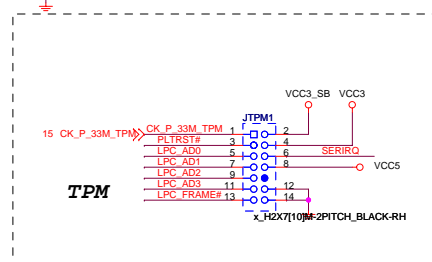
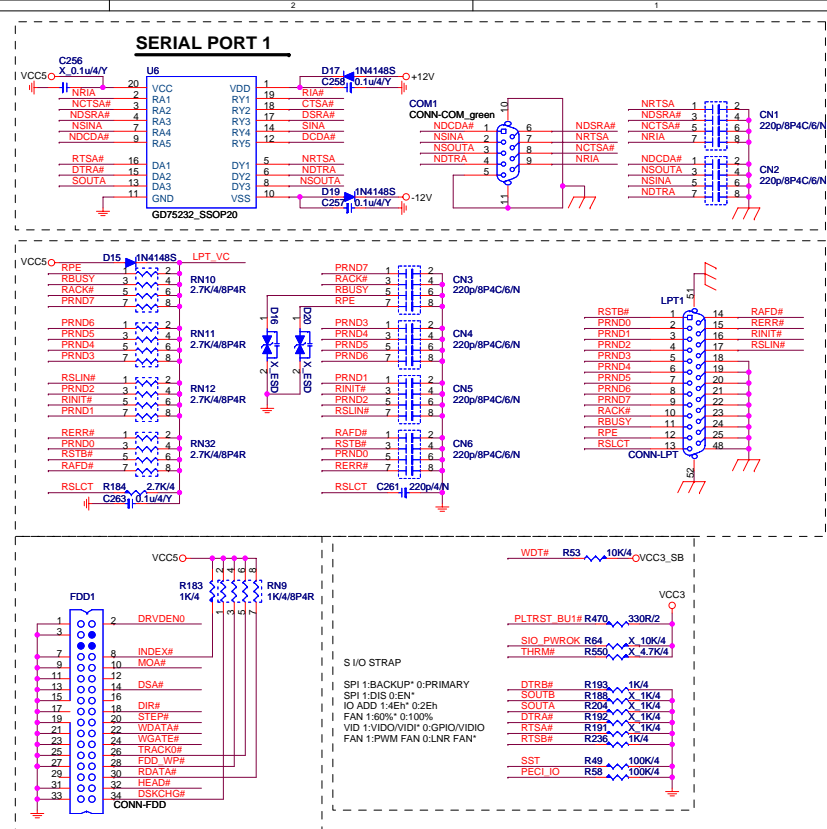
### Optics Orientation Holes



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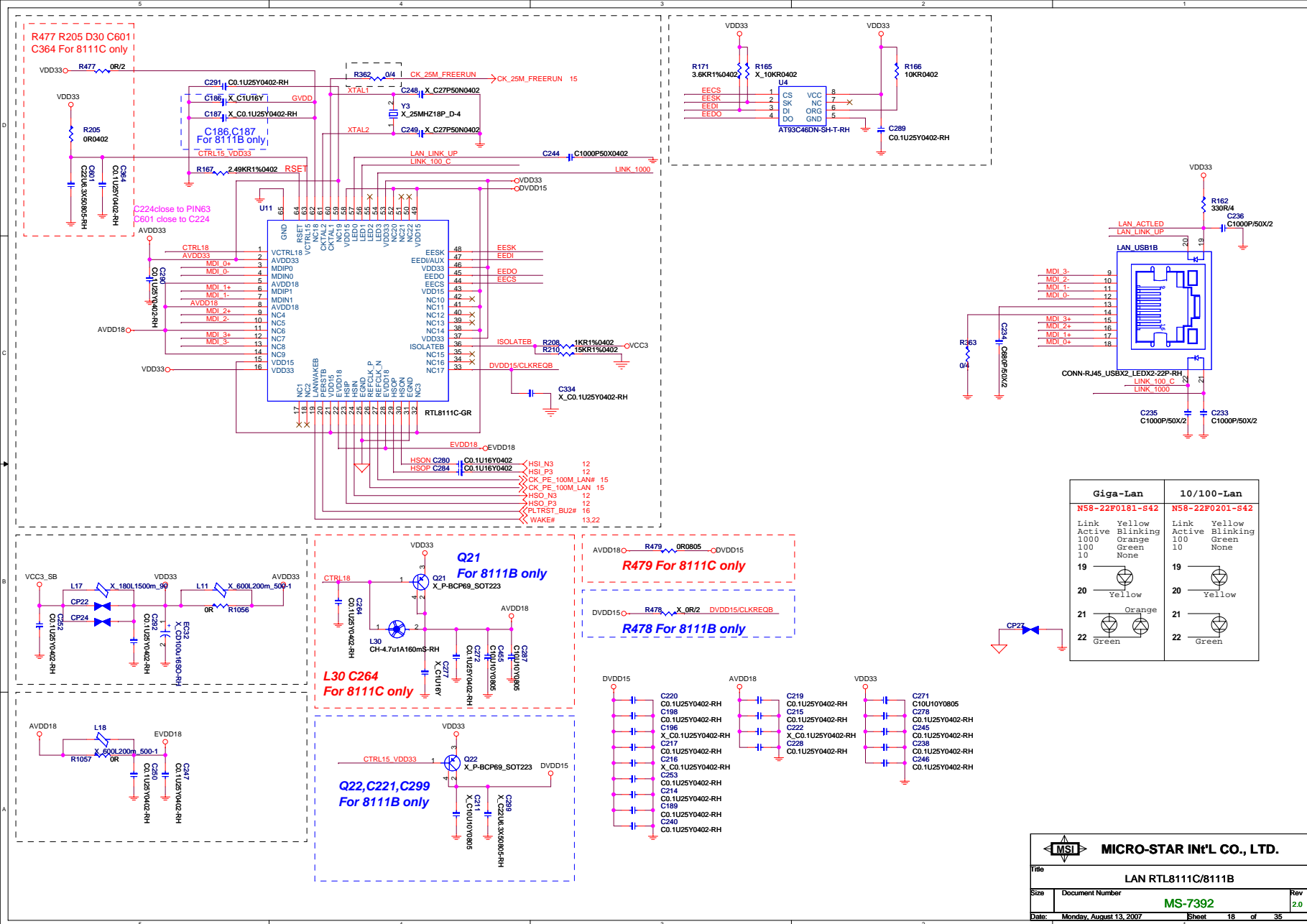
Title				Clock - ICS9LPRS906CGLF			
Size	Document Number						Rev
	MS-7392						2.0
Date:	Friday, August 10, 2007			Sheet	15	of	35








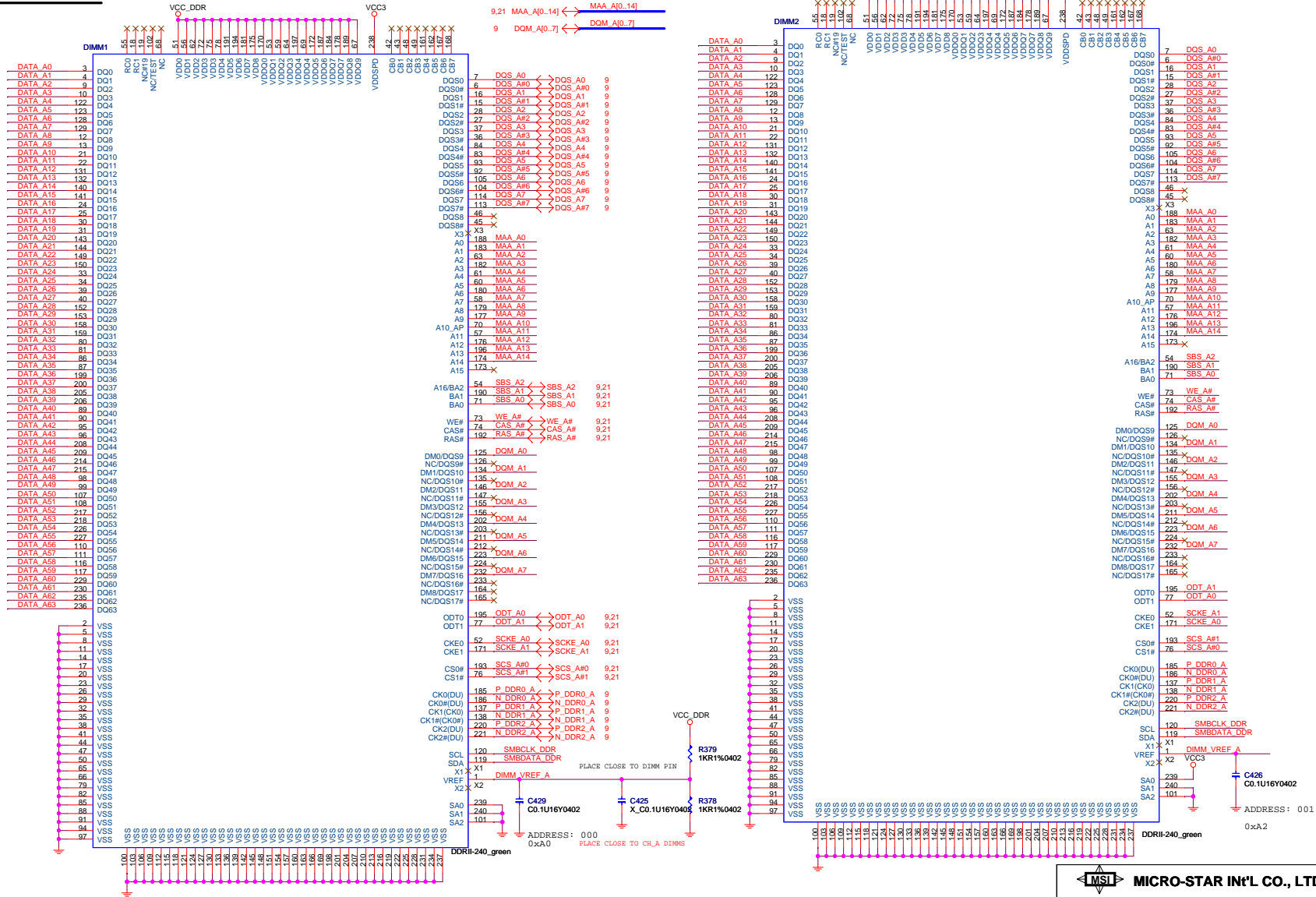






Giga-Lan		10/100-Lan	
<b>N58-22P0181-S42</b>		<b>N58-22P0201-S42</b>	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	Yellow	20	Yellow
21	Orange	21	
22	Green	22	Green

## DDR2 CHANNEL A

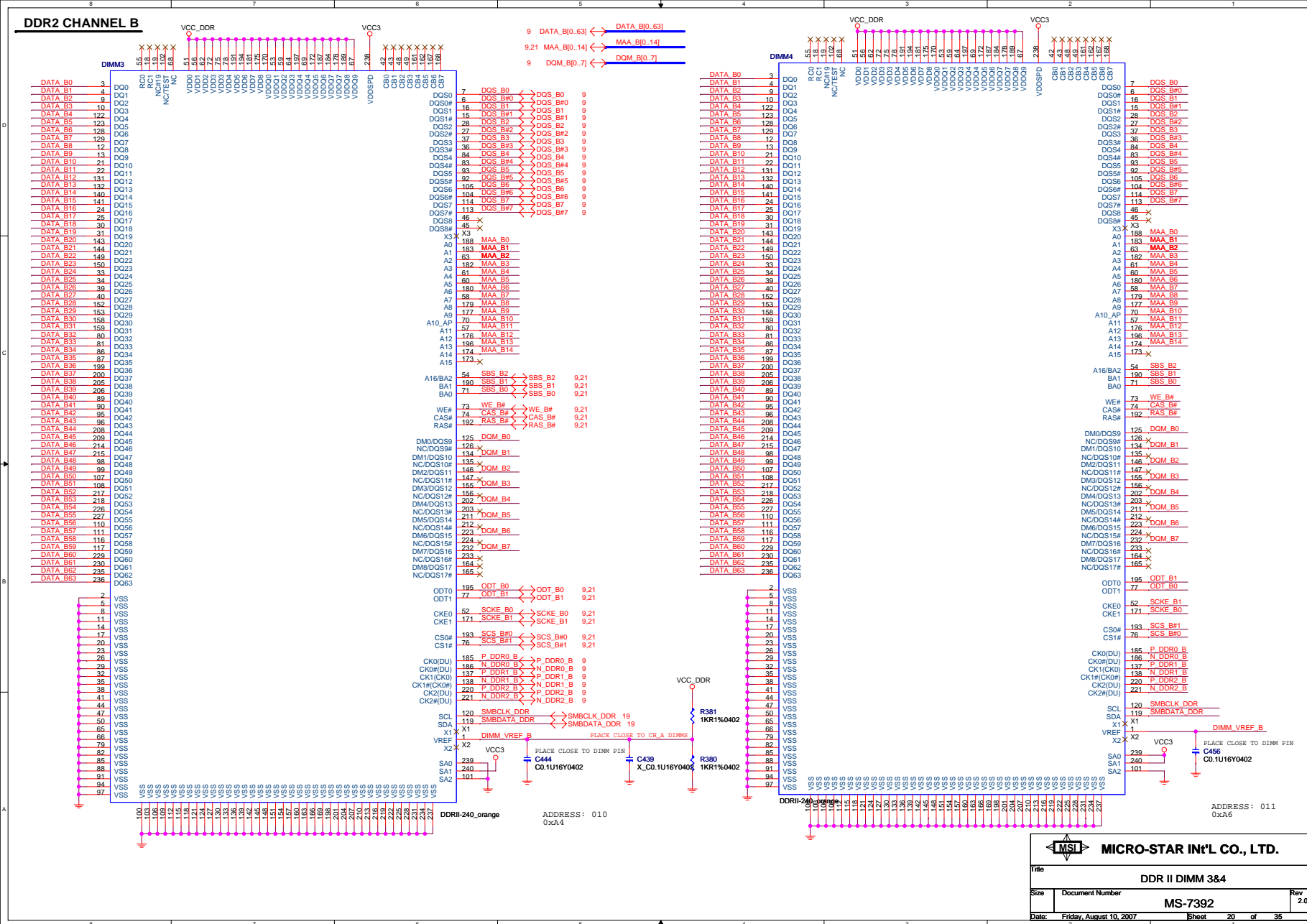


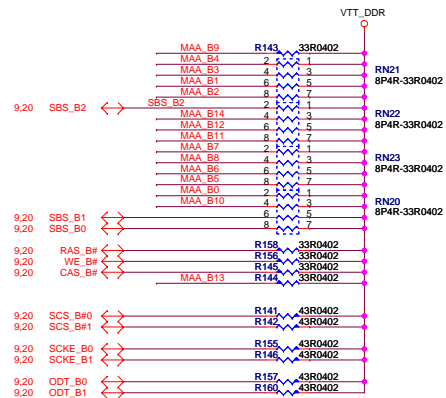
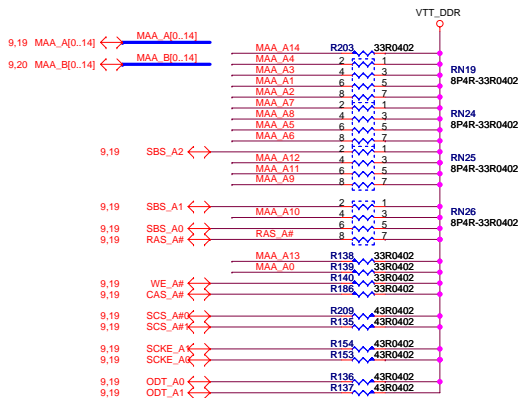
► **MICRO-STAR INT'L CO., LTD.**

DDR II DIMM 1&amp;2

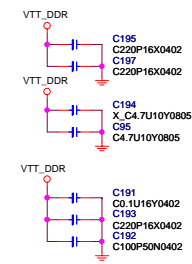
Size	Document Number	Rev
	MS-7392	2.0
Date:	Friday, August 10, 2007	Sheet 19 of 35

## DDR2 CHANNEL B

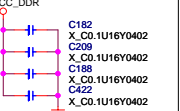
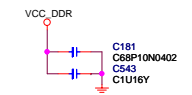
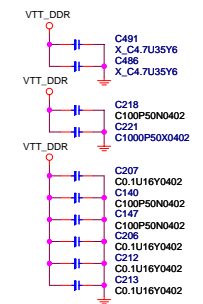




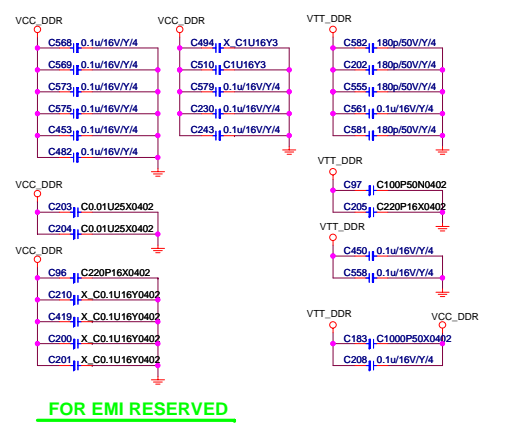
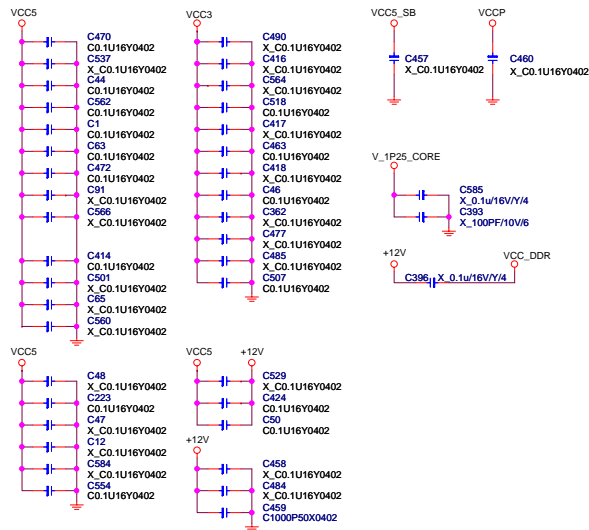
CHANNEL A V\_SM\_VTT DECOUPLING CAPS



CHANNEL B V\_SM\_VTT DECOUPLING CAPS



FOR EMI RESERVED

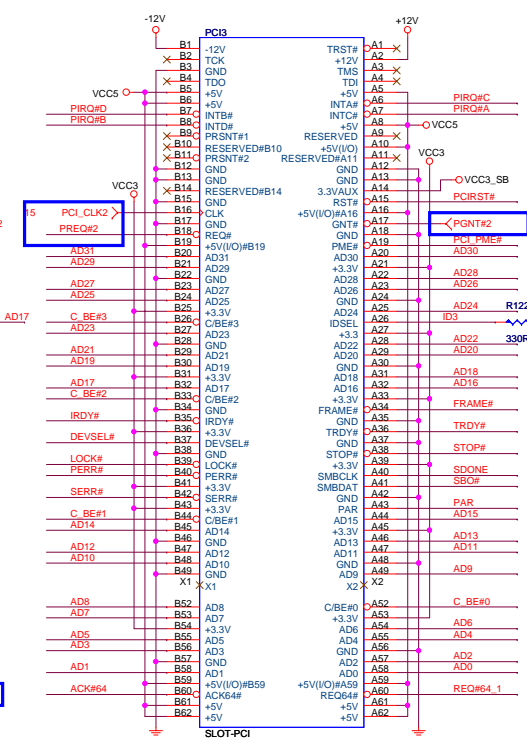


FOR EMI RESERVED

MICRO-STAR INT'L CO., LTD.		
DDR II VTT DECOUPLING		
Size	Document Number	Rev
	MS-1032	2.0
Date:	Friday, August 10, 2007	Sheet 21 of 35



PCI SLOT 3 (PCI VER: 2.2 COMPLY

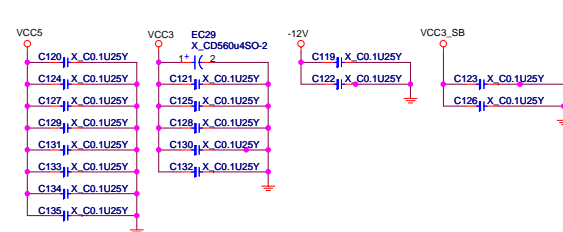


```

IDSEL = AD18
MASTER = PREQ#2
PIRQ#C

```

## PCI SLOT DECOUPLING CAPACITORS

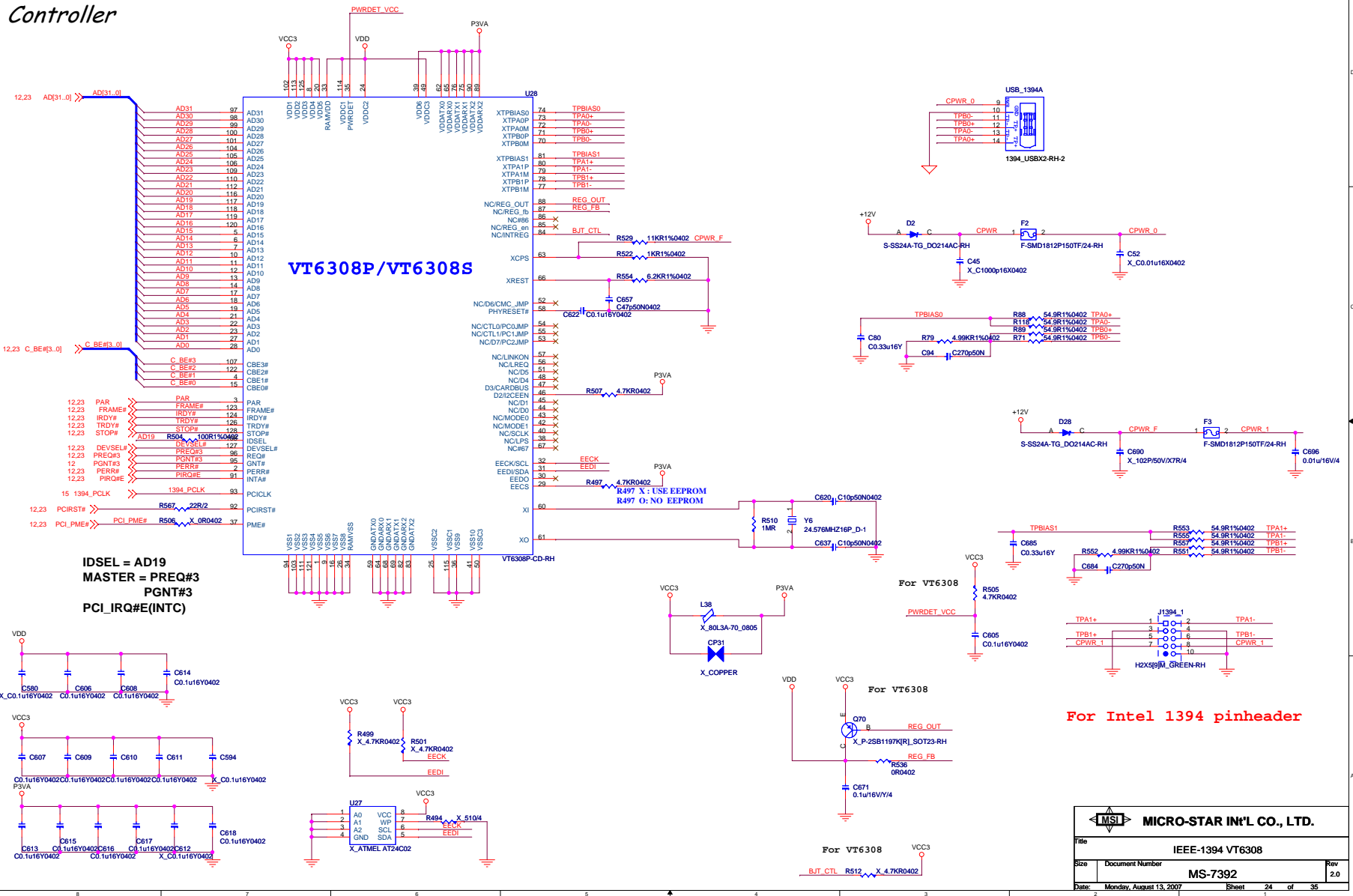


Title			
PCI 1~ 4 Slots			
Size	Document Number	Rev	
	MS-7392	2.0	
Date	Friday, August 10, 2007	Sheet	23 of 35



# 1394a OHCI Link Layer Controller

## Controller



For Intel 1394 pinheader

MICRO-STAR INT'L CO., LTD.		
Title IEEE-1394 VT6308		
Size Document Number MS-7392		Rev 2.0
Date Monday, August 13, 2007		Sheet 24 of 35



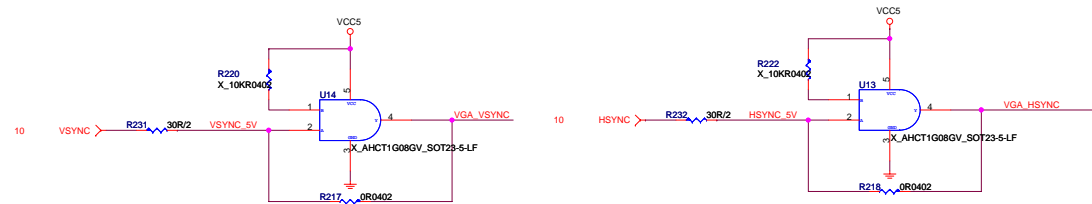
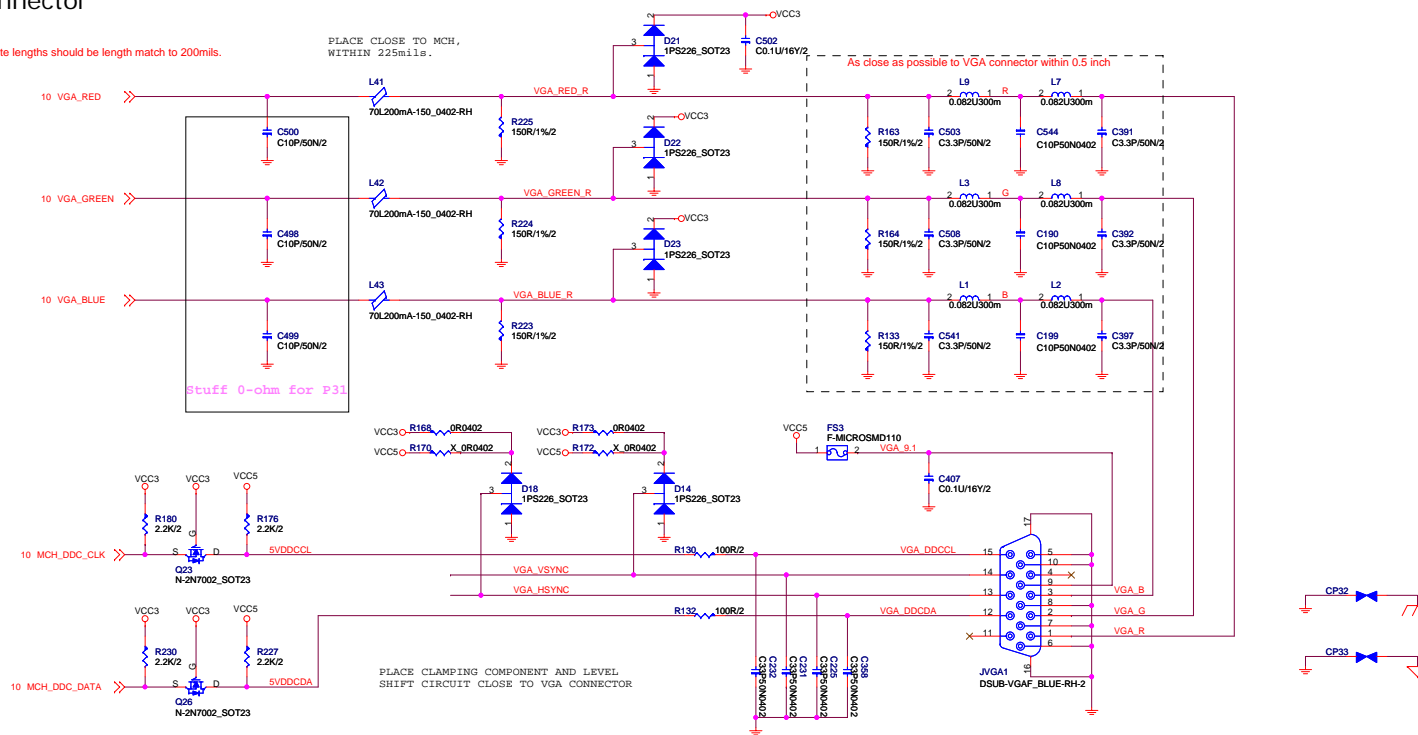
## Video Connector

Thw R ,G ,B route lengths should be length match to 200mils.

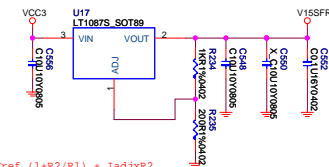
PLACE CLOSE TO MCH,  
WITHIN 225mils.

PLACE CLOSE TO VGA CONNECTOR

As close as possible to VGA connector within 0.5 inch



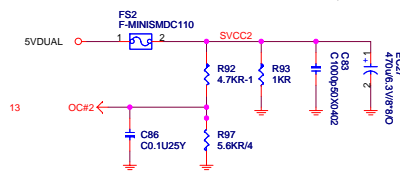
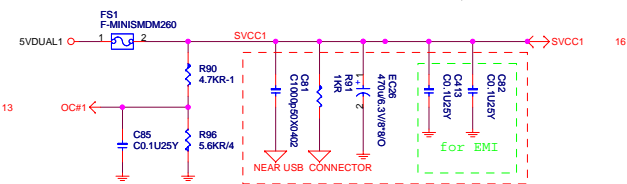
$V_o = V_{ref} (1 + R_2/R_1) + I_{adj} R_1$   
where  $V_{ref} = 1.25V$ ,  $I_{adj} = 55\mu A$



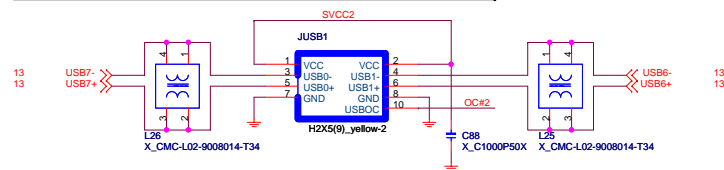
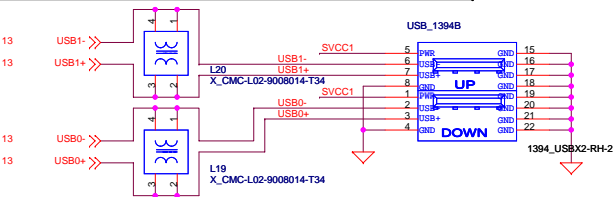
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Title			
ATA33/66/100 IDE & SATA Connectors			
Size	Document Number	Rev	
	MS-7392	2	
Date:	Monday, August 13, 2007	Sheet	25 of 35

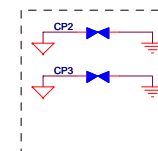
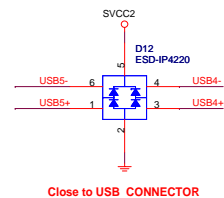
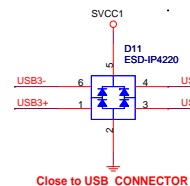
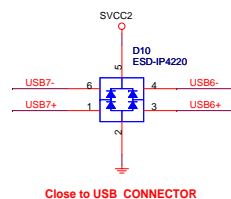
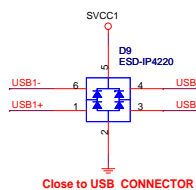
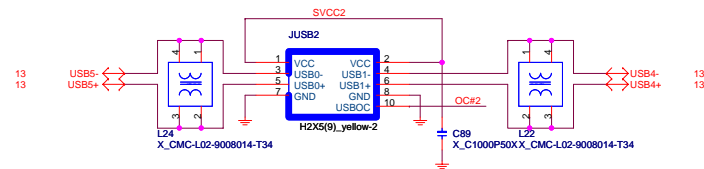
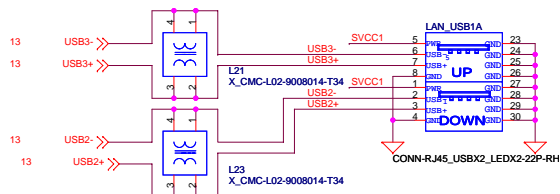
### POWER CIRCUIT FOR USB PORT (FRONT)



### FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

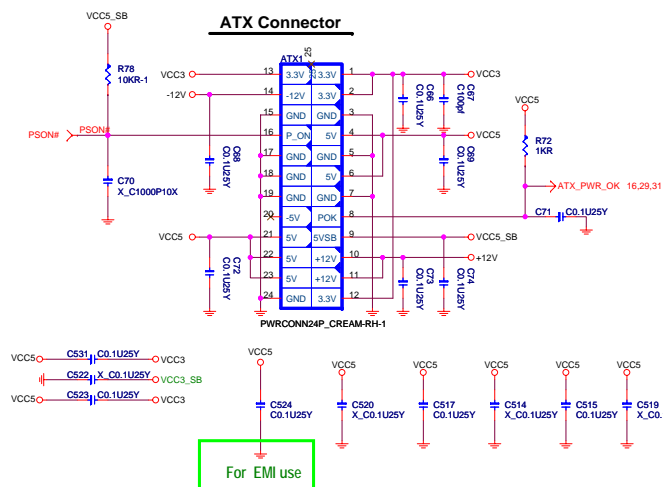


### FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

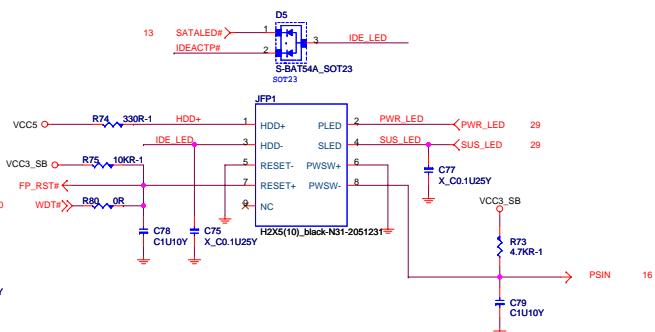


## USB Connectors

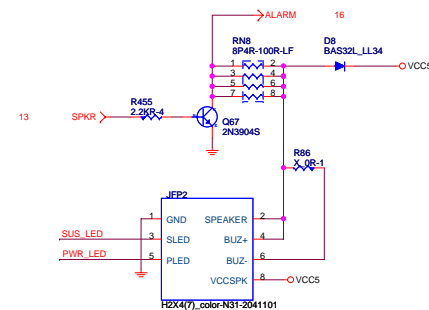
Title				
USB Connectors				
Size	Document Number	MSM3-7392		Rev 2.0
Date:	Friday, August 10, 2007	Sheet	26	of 35



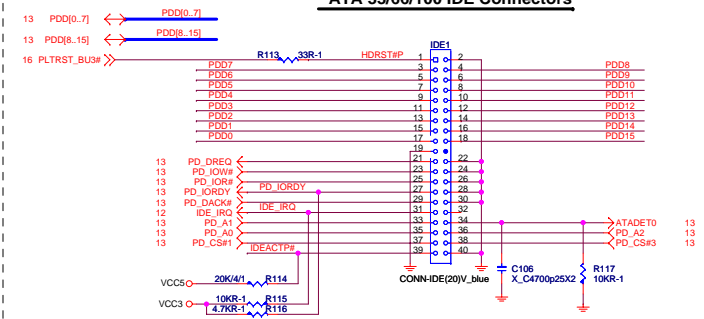
### INTEL/PB Front Panel Connector



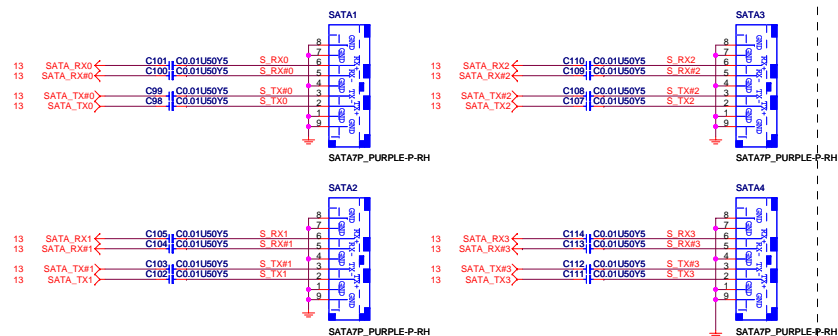
### MSI Front Panel Connector



### ATA 33/66/100 IDE Connectors



## SERIAL ATA CONNECTOR BLOCK



**MICRO-STAR INT'L CO., LTD.**

Title

### ATX Connector & Front Panel

Size

Document Number

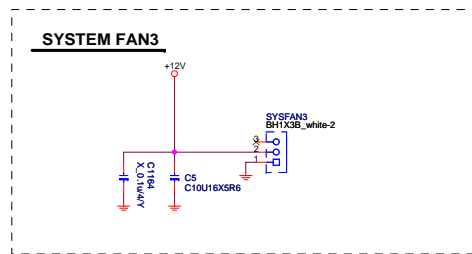
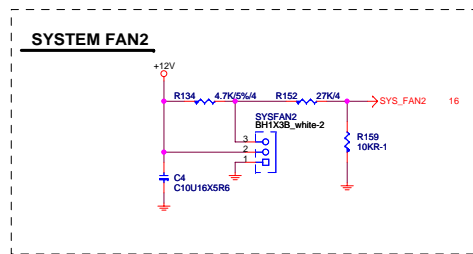
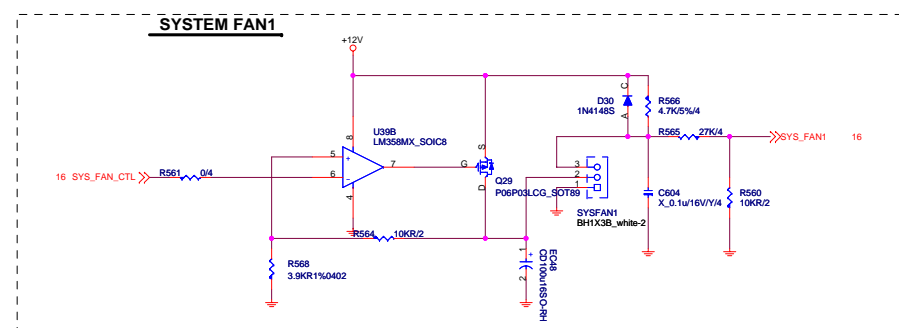
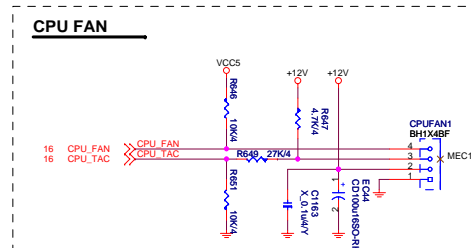
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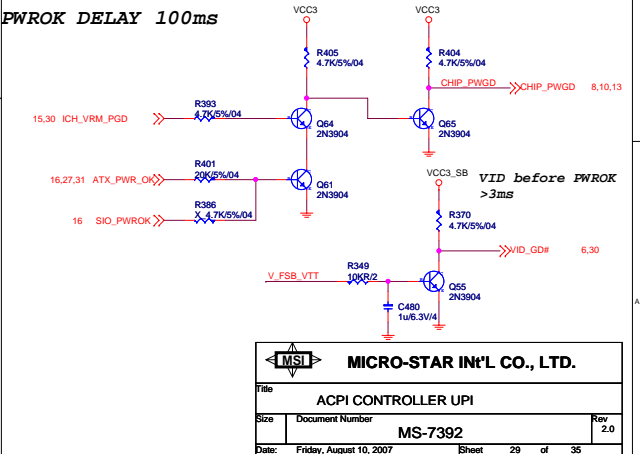
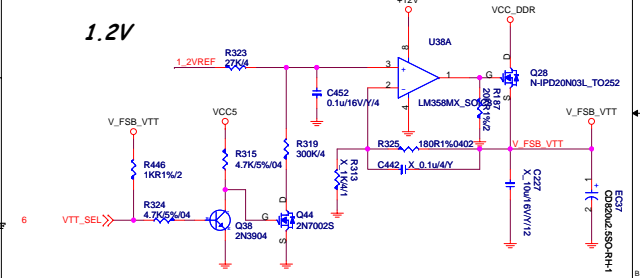
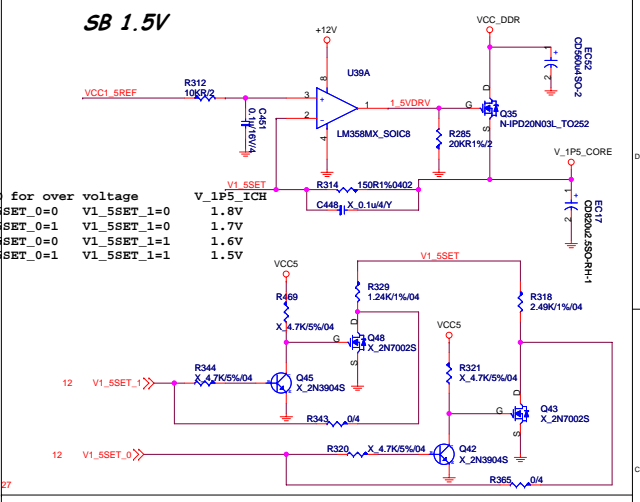
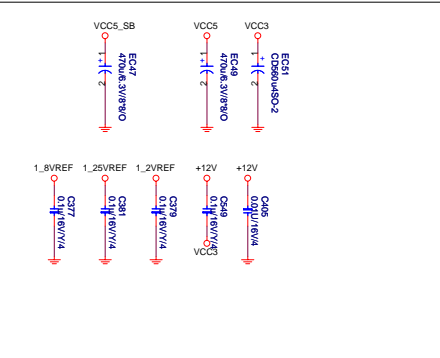
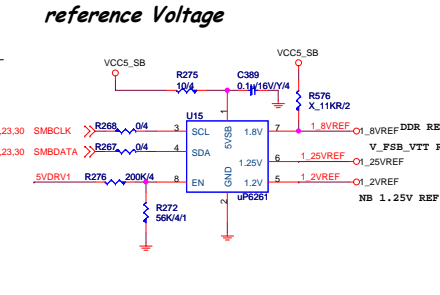
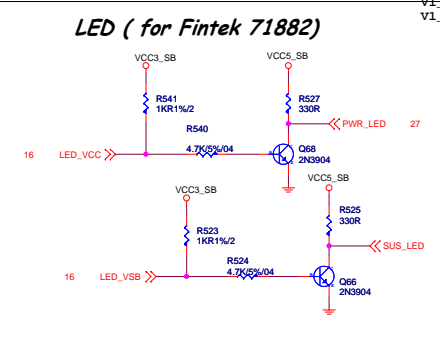
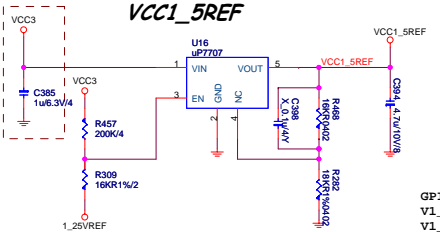
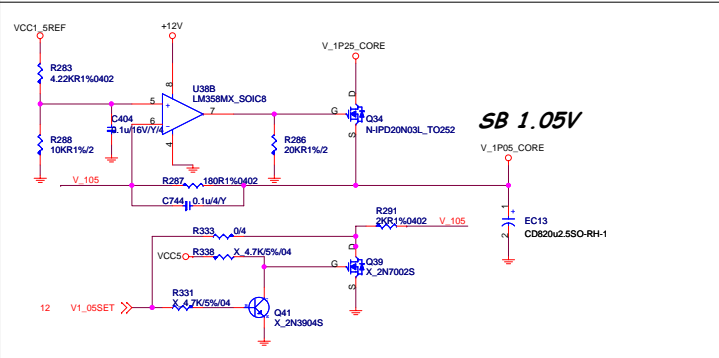
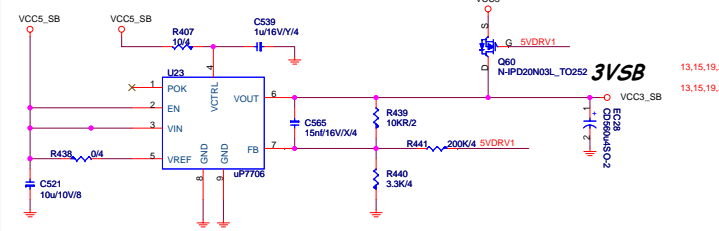
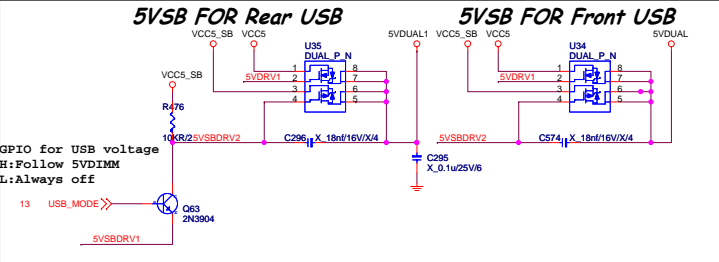
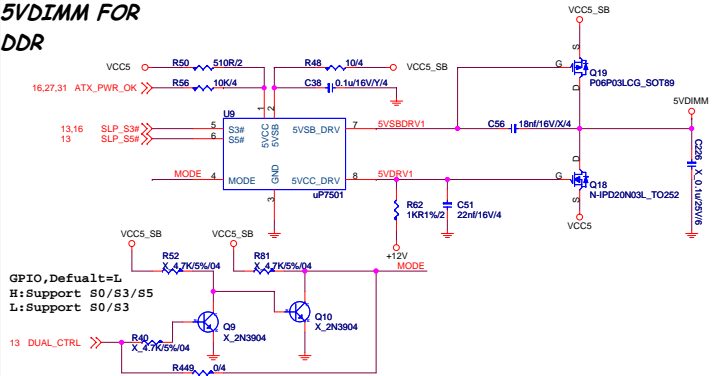
Rev

Date: Friday, August 10,

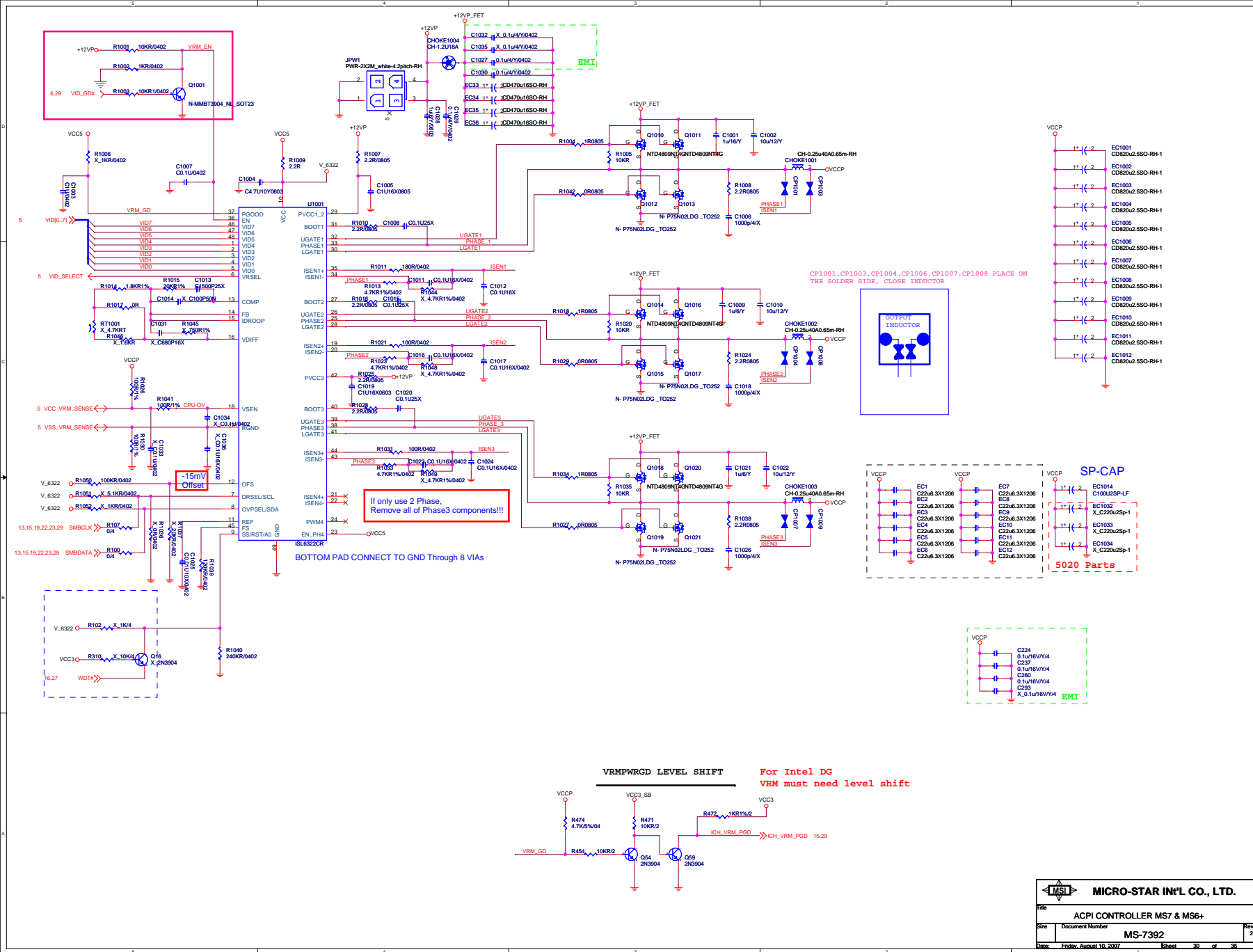
Sheet

27 of 3

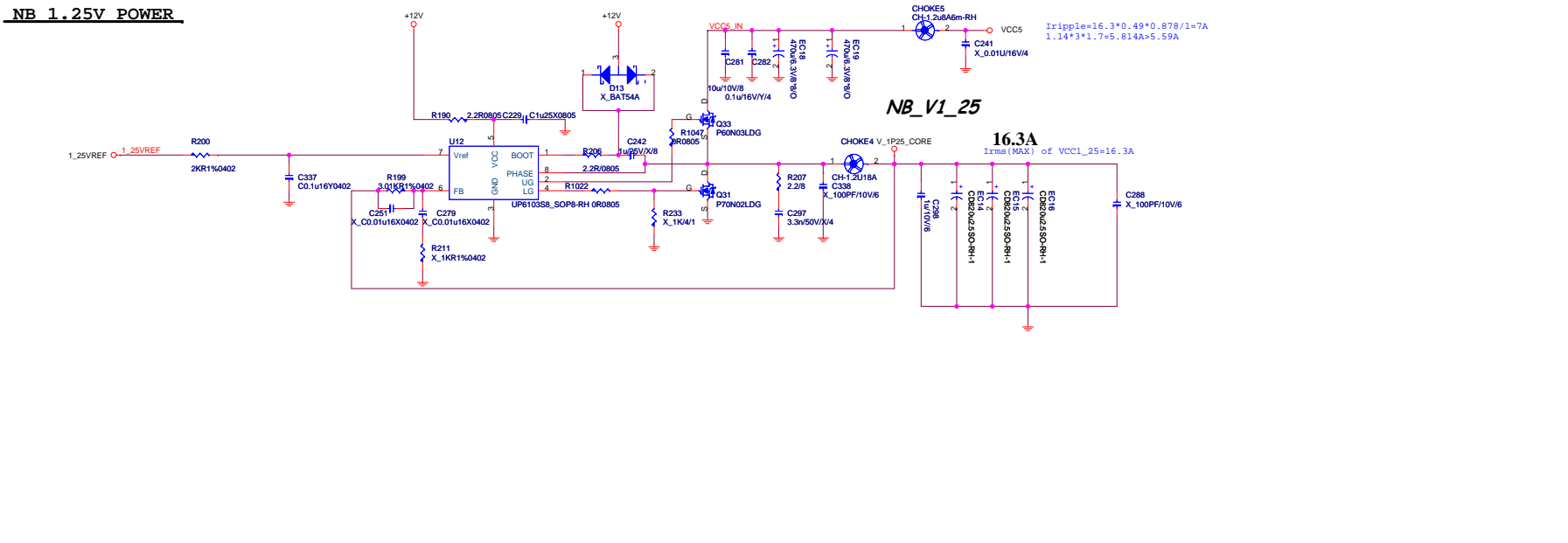




MICRO-STAR INT'L CO., LTD.		
Title	ACPI CONTROLLER UPI	
Size	Document Number	Rev
	MS-7392	2.0
Date:	Friday, August 10, 2007	Sheet 29 of 35



NB 1.25V POWER



## Auto-BOM Manual Parts

PCB1  
PCB  
PCB-7392

BATTERY1  
BATTERY-CR2032

## Auto-BOM Option Parts

RTL8111B  
OPT  
X\_RTL8111B

ICH7R  
OPT  
X\_ICH7R

G31  
OPT  
X\_G31

P31-R1  
OPT  
X\_OR0402

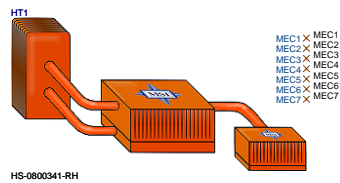
OnVGA1.3  
OPT  
X\_1.3KR1%/2

G31-C1  
OPT  
X\_C0.1U16V0402

P31 HEATSINK ICH7 HEATSINK

P31 HEATSINK  
OPT  
P31 HEATSINK

ICH7 HEATSINK  
OPT  
ICH7 HEATSINK



MEC1 X MEC1  
MEC2 X MEC2  
MEC3 X MEC3  
MEC4 X MEC4  
MEC5 X MEC5  
MEC6 X MEC6  
MEC7 X MEC7



MICRO-STAR INT'L CO., LTD.

Title AutoBOM		
Size	Document Number MS-7392	Rev 2.0
Date Monday, August 13, 2007	Sheet 32	of 35



- 54321
- 0A Change 1.0 list:
1. Modify VCCA\_EXP pullup VCC3 (page 10);
2. Modify USB 5vdual N-MOS to P-MOS (page 29);
3. Modify ICH7 VRM\_PWRGD sequence (page 13);
4. Change LAN to RTL8111C CO-LAY RTL8111B (page 18);
5. Add EC28 FOR SYSTEM FAN2 (page 28);
6. Change PCI-SLOT pull up power VCC5 to VCC3 (page 23);
- D
- C
- B
- A
- 54321

Title		
<Title>		
Size	Document Number	Rev
A	MS-7392	2.0
Date:	Tuesday, August 07, 2007	Sheet 33 of 35

54321

ICH7									
GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	PIRQ#E
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	PIRQ#F
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	PIRQ#G
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	PIRQ#H
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	JAUD2_EN#
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	SMB_ALERT#
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	0	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	N/A	PGNT#5
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	1	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	1	NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	PREQ#4
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC (NO CHANGE)
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	1	NC
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	0	NC
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	0	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	0	NC
GPIO29	DC5#	C3	I/O	Resume	N	N	3.3V	GPI	OC#2
GPIO30	DC6#	A2	I/O	Resume	N	N	3.3V	GPI	OC#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	OC#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	1	BIOS_WP#
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	1	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	0	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	1	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	PGNT#4
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD
Following are the GPIOs that need to be terminated properly if not used: GPIO[39;36;23;21;19;7;0]; default as inputs and should be pulled up to Vcc3_3 if unused. GPIO[31;29;15;8]; default as inputs and should be pulled up to VccSus3_3 if unused.									

SIO W83627EHF(CONTINUE)				
GPIO	Alt Func	PIN	USAGE	Input/Output
GP44	DTRB#	81	DTRB#	OUT8
GP45	RTSB#	80	RTSB#	OUT8
GP46	DSRB#	79	DSRB#	INt
GP47	CTSB#	78	CTSB#	INt
GP50	EN_VRM10/WDTO#	77	STRAPPED DOWN	INcd
GP51	RSMRST#	75	RSMRST#	OD12
GP52	SUSB#	73	SLP_S3#	INt
GP53	PSON#	72	PSON#	OD12
GP56	PSIN	68	PSIN	INId
GP57	PSOUT#	67	PSOUT#	OD12
GP60	RIA#	57	RIA#	INt
GP61	DCDA#	56	DCDA#	INt
GP62	SOUTA/PENKBC	54	SOUTA	OUT8
GP63	SINA	53	SINA	INt
GP64	DTRA#PENROM	52	DTRA#	OUT8
GP65	RTSA#HEFRAS	51	RTSA#	OUT8
GP66	DSRA#	50	DSRA#	INt
GP67	CTSA#	49	CTSA#	INt

GPIO	PIN	POWER	TOL	SIGNAL NAME
FGPIO0	6	MAIN	3.3V	ATADET0
FGPI1	5	MAIN	3.3V	PULL UP
FGPI2	4	MAIN	3.3V	PULL UP
FGPI3	3	MAIN	3.3V	PULL UP
FGPI4	30	MAIN	3.3V	PULL DOWN

Note: FWH GPs should only be used for static options, do not put dynamic nets on these

PCI Config.				
DEVICE	MCPI INT	REQ#/GNT#	IDSEL	CLOCK
LAN	PIRQ#E	PREQ#4 PGNT#4	AD20	PCI_LAN
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1
PCI3	PIRQ#C PIRQ#D PIRQ#A PIRQ#B	PREQ#2 PGNT#2	AD18	PCI_CLK2
PCI4	PIRQ#D PIRQ#A PIRQ#B PIRQ#C	PREQ#3 PGNT#3 PREQ#5 PGNT#5	AD19 AD21	PCI_CLK3 PCI_CLK4

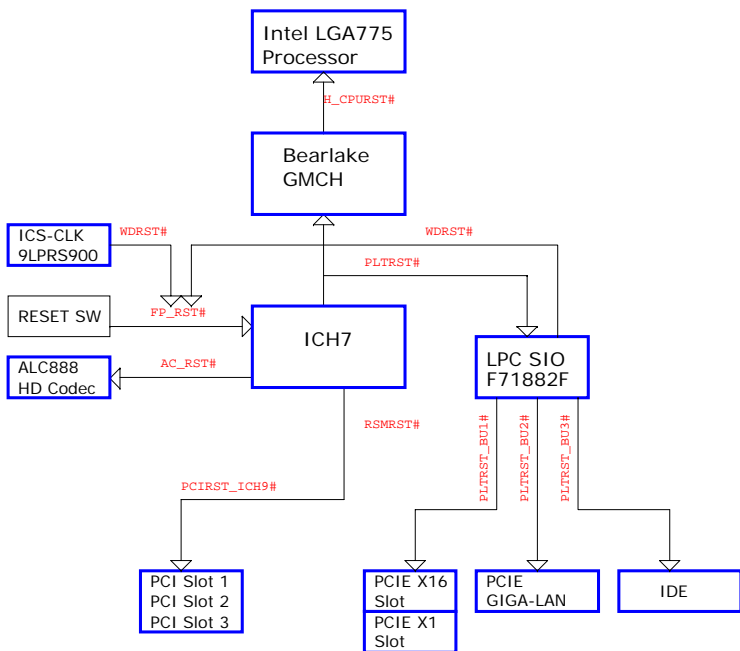
DDRII DIMM Config.		
DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM 2	A2H	P_DDR3_A/N_DDR3_A P_DDR4_A/N_DDR4_A P_DDR5_A/N_DDR5_A
DIMM 3	A4H	P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B
DIMM 4	A6H	P_DDR3_B/N_DDR3_B P_DDR4_B/N_DDR4_B P_DDR5_B/N_DDR5_B

JUMPER SETTING		
JBAT1	(1-2)NORMAL	(2-3)CLEAR

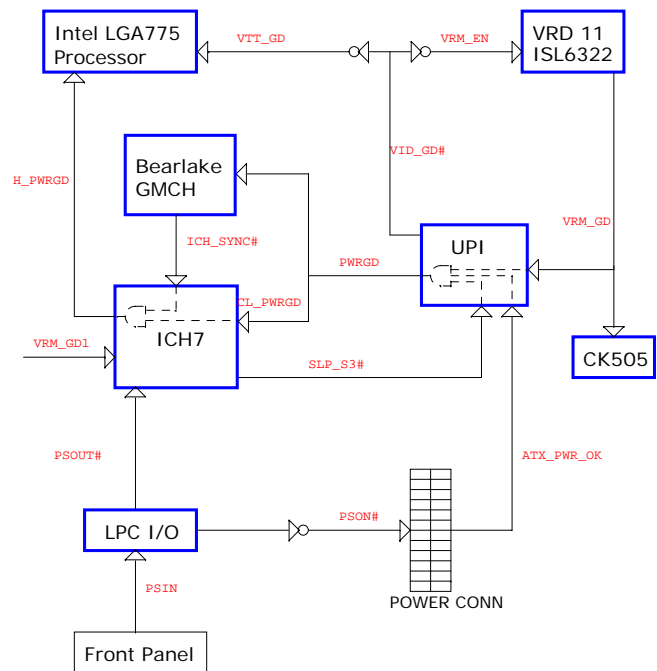
JCI1	Chassis Intrusion
Open	Normal
(1-2)	Chassis Open

GPIO MAP & JUMPER SETTING		
REV	Document Number	Rev
	MS-7382	2.0
Date	Thursday, August 07, 2008	Sheet 34 of 35

## RESET MAP



## PWROK MAP



Title			
POWEROK MAP			
Size	Document Number		Rev
	MS-7392		2.
Date:	Tuesday, August 07, 2007	Sheet	35 of 35